Monthly Report for

12-Bit High Dynamic Range ADC

Reporting Period: 15 December 1999 to 15 January 2000

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1.0 Technical Progress

During this reporting period, assembly of engineering prototype MCMs was completed and MCM debugging performed.

Figure 1 shows a photograph of a completely assembled MCM. Figure 2 is a corresponding block diagram which illustrates the electrical contents of the 2" x 1.5" ceramic module. Significant effort was required to completely debug the ADC and calibration circuitry. The primary problem turned out to be improper voltage biasing of the Cal DAC and EEPROM die. This was rectified by inserting a ceramic spacer under each of these die and bonding to the proper voltage (in the case of the CAL DACs), or left floating (in the case of the EEPROM). Other minor problems encountered included MCM test fixture solder shorts and non-optimal FPGA die programming procedures. Fully functional ADC MCMs have been achieved, and performance characterization of engineering prototypes is in progress.

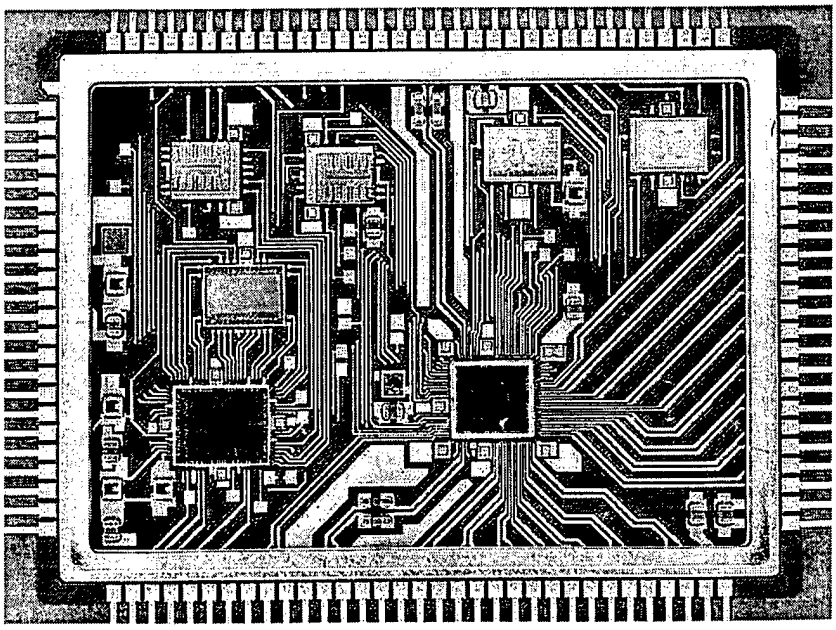

Figure 1. Photo of Assembled ADC MCM (2" x 1.5")

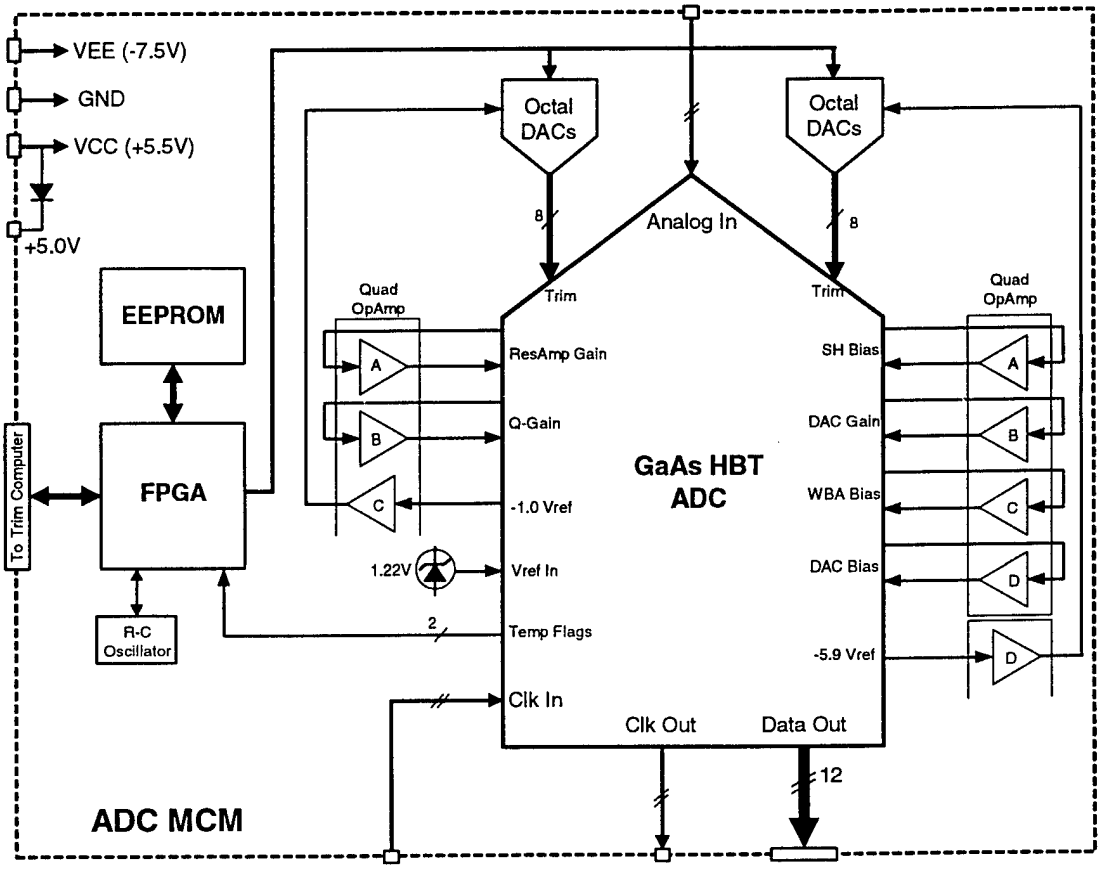

Figure 2. Block Diagram of ADC MCM (9 active + 40 passive components).

2. Plans for Next Reporting Period

During the next reporting period, performance characterization of engineering prototype MCMs will be completed, and assembly and test of the deliverable MCMs initiated.

3. Financial Status

Table 1 shows the forecasted versus actual expenditures for the Phase 2 program. At month-end November, 1999 the cumulative actuals were $589.2K versus a forecast of $657.0K (an underrun of $68K). This underrun reflects the MCM schedule slip which has delayed the MCM test activities.

Table 1. Phase 2 Expenditures Forecast

Month	Monthly Total ($K)	Cumulative Total ($K)	Cumulative Actuals ($K)	Delta (Forecast - Actuals)
Mar-99	65.0	65.0	56.9	8.1
Apr-99	109.4	174.4	133.0	41.4
May-99	100.8	275.2	191.2	84.0
Jun-99	107.5	382.7	275.1	107.6
Jul-99	45.9	428.6	356.1	72.5
Aug-99	32.1	460.7	401.5	59.2
Sep-99	79.6	540.3	425.6	114.7
Oct-99	74.6	614.9	505.7	109.2
Nov-99	27.0	641.9	545.2	96.7
Dec-99	15.1	657.0	589.2	67.8

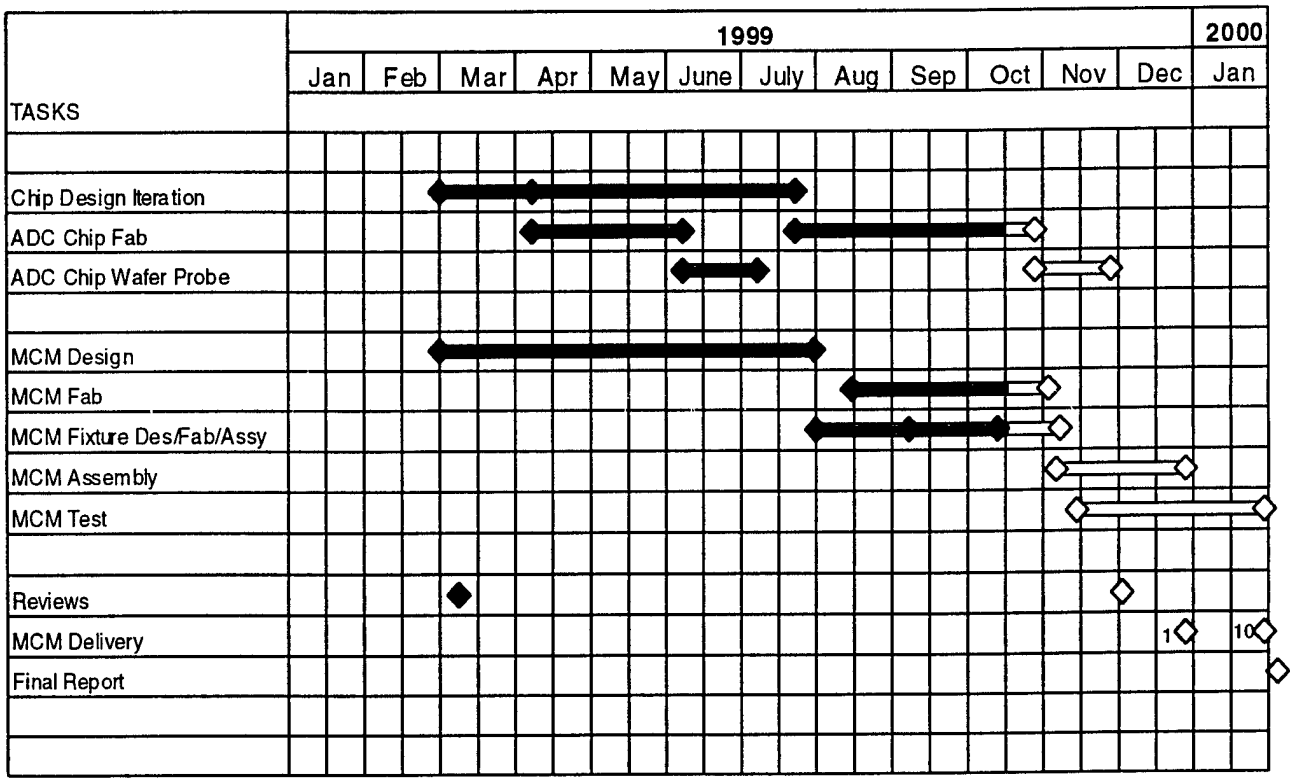

Figure 4. Development Schedule for Phase 2 Activities.